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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/725,862	11/30/2000	Stephen E. Greco	00750414BA	3056

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EXAMINER
NGUYEN, JOSEPH H

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No. 09/725,862	Applicant(s) GRECO ET AL.	
	Examiner Joseph Nguyen	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-33 and 36-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-33 and 36-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 27 and 38 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The phrase "a flowable oxide layer formed of a flowable oxide material having a lower dielectric constant than SiO2" is not supported by the specification and thus is deemed to be new matter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27, 31-33, 36-41, 43-46, 49, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawanoue et al in view of Cohen et al.

Regarding claim 27, Kawanoue et al discloses on figure 24 an integrated circuit semiconductor device including a substrate having a substrate surface, a flowable oxide

insulator (FOX) layer 161 upon said substrate surface, a trough 165 in said flowable oxide insulator layer, sidewalls of said flowable oxide insulator layer, a primary protective layer 163 on said sidewalls of said flowable oxide insulator layer, said primary protective layer being a thin oxidized surface of said FOX flowable oxide insulator material on said sidewalls within said trough, said thin surface layer preventing the exposure of said flowable oxide insulator layer to moisture and lithographic resist developers, said primary protective layer being substantially impervious to copper extrusion, and a secondary protective layer 164 on said primary protective layer and on said substrate surface, said secondary protective layer being electrically conductive.

Kawanoue et al does not disclose a flowable oxide FOX insulator layer formed of a flowable oxide material having a lower dielectric constant than SiO2. However, Cohen et al discloses on figures 1 a flowable oxide FOX insulator layer 1 formed of a flowable oxide material having a lower dielectric constant than SiO2. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawanoue et al by having a flowable oxide FOX insulator layer formed of a flowable oxide material having a lower dielectric constant than SiO2 for the purpose of providing excellent gap fill capability in a semiconductor device as taught by Cohen et al (col. 1, lines 51-52).

Regarding claim 31, Kawanoue et al discloses on figure 24 a nitride supplemental protective layer 166 on said primary protective layer for improving adhesion with a metallic conductor.

Regarding claim 32, Kawanoue et al discloses on figure 24 said primary layer is a barrier layer.

Regarding claim 33, Kawanoue et al discloses on figure 24 said primary protective layer 163 on said sidewalls of said flowable insulator 161 has a thickness equal to or less than 20% of thickness of said flowable oxide insulator layer (col. 20, line 63 and col. 21, lines 24-25).

Regarding claim 36, Kawanoue et al discloses on figure 24 said supplemental protective layer 166 is a nitride layer.

Regarding claim 37, Kawanoue et al discloses on figure 24 said thin layer of oxide has a thickness not exceeding about 500 A.

Regarding claim 38, Kawanoue et al discloses on figure 24 an integrated circuit including a layer of flowable oxide insulator 161, and a thin protective layer 163 thereon, said thin protective layer being an oxidized surface layer of said flowable oxide insulator that is resistant to moisture and lithographic resist developers.

Kawanoue et al does not disclose a flowable oxide FOX insulator layer formed of a flowable oxide material having a lower dielectric constant than SiO2. However, Cohen et al discloses on figures 1 a flowable oxide FOX insulator layer 1 formed of a flowable oxide material having a lower dielectric constant than SiO2. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawanoue et al by having a flowable oxide FOX insulator layer formed of a flowable oxide material having a lower dielectric constant than SiO2 for the purpose

of providing excellent gap fill capability in a semiconductor device as taught by Cohen et al (col. 1, lines 51-52).

Regarding claim 39, Kawanoue et al discloses on figure 24 said thin oxidized layer 161 ha a thickness less than about 500 A (col. 21, lines 24-25).

Regarding claim 40, the claim limitation is merely the product by process and therefore not given patentable weight.

Regarding claim 41, Kawanoue et al discloses on figure 24 a nitride or oxide nitride layer 166 on said thin oxidized surface layer 163.

Regarding claim 43, Kawanoue et al discloses on figure 24 a conductive layer 164 on said thin oxidized surface layer 163.

Regarding claim 44, Kawanoue et al discloses on figure 24 a metal conductor 165 in contact with said conductive layer 164.

Regarding claim 45, Kawanoue et al discloses on figure 24 said metal conductor 165 contains copper.

Regarding claim 46, Kawanoue et al discloses on figure 24 said conductive barrier layer 164 includes a refractory metal or alloy.

Regarding claims 49 and 51, the claim language is merely product by process and therefore is not given a patentable weight.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawanoue et al and Cohen et al as applied to claim 27 above, and further in view of Lopatin et al.

Regarding claim 28, Kawanoue et al and Cohen et al disclose substantially all the structure set forth in the claimed invention except an oxidized FOX layer on a surface of said FOX layer and an oxide layer upon said oxidized FOX layer. However, Lopatin et al disclsoses on figure 2 an oxidized FOX layer 105 on a surface of said FOX layer 108 and an oxide layer 108 upon said oxidized FOX layer 116. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawanoue et al and Cohen et al by having an oxidized FOX layer on a surface of said FOX layer and an oxide layer upon said oxidized FOX layer for the purpose of effectively establishing the electrical interconnects in the integrated circuit semiconductor device.

Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawanoue et al and Cohen et al and Lopatin et al as applied to claim 28 above, and further in view of Yew et al.

Regarding claims 29 and 30, Kawanoue et al and Cohen et al and Lopatin et al disclose substantially all the structure set forth in the claimed invention except the integrated circuit semiconductor device comprising a second damascene layer. Note that the second damascene layer is merely duplication of the first damascene layer of claim 27. However, Yew et al discloses on figure 2E the second damascene layer 226, 212 similar to the first damascene layer 222, 204. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawanoue et al and Cohen et al and Lopatin et al by having the second

damascene layer similar to the first damascene layer in the integrated circuit semiconductor device. The ordinary artisan would have been motivated to modify Kawanoue et al and Lopatin et al in the manner described for the purpose of having a reduced parasite capacitance in the dielectric layers, thus assuring the performance of an IC device (col. 3, line 15-18).

Claims 42, 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawanoue et al and Cohen et al as applied to claim 46 above, and further in view of Usami.

Regarding claims 42 and 47, Kawanoue et al discloses on figure 24 substantially all the structure set forth in the claimed invention except the layer of flowable oxide insulator being located between two non-coplanar metal layers. However, Usami discloses on figure 1 the layer of flowable oxide insulator 4 being located between two non-coplanar metal layers 3. In view of such teaching, it would have been obvious to one of ordinary skill in that art at the time the invention was made to modify Kawanoue et al and Cohen et al by having the layer of flowable oxide insulator being located between two non-coplanar metal layers for the purpose of effectively establishing the electrical interconnects within the integrated circuit device.

Regarding claim 48, Kawanoue et al and Cohen et al and Usami together disclose the structure of claim 48.

Claims 50 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawanoue et al and Cohen et al as applied to claims 27 and 38 above.

Regarding claims 50 and 52, Kawanoue et al and Cohen et al disclose substantially all the structures set forth in the claimed invention except said primary protective layer having a thickness less than approximately 20% of a thickness of said flowable oxide insulator layer. However, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify Kawanoue et al and Cohen et al by having said primary protective layer having a thickness less than approximately 20% of a thickness of said flowable oxide insulator layer for the purpose of providing excellent gap fill capability in a semiconductor device, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

Applicant's arguments with respect to claims 27 and 38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
April 16, 2003

EDDIE LEE
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